Dual-Channel Trench-Gate (DCTG) Tunnel FET for Improved ON-current and subthreshold Swing

Tripuresh Joshi, Y Singh and Balraj Singh

In this paper, a dual-channel trench-gate tunnel FET (DCTG-TFET) is proposed and investigated. The gate of DCTG-TFET is placed vertically in a trench to create two channels which carry drain current in parallel. The proposed device dimensions are optimized to reduce channel resistance and tunnelling width for appreciable increase in ON-state current (I_{ON}). The performance of DCTG-TFET is analysed using two-dimensional simulations in the device simulator (ATLAS). The proposed DCTG-TFET provides one order of magnitude improvement in I_{ON}/I_{OFF} current ratio and seventeen times reduction in subthreshold swing (SS) as compared to recently reported two-source-region (TRS) TFET structure.

Introduction: The indefinite scaling of supply voltages in the conventional metal-oxide-semiconductor field-effect transistors (MOSFET) causes performance degradation which restricts the further scaling of threshold voltage (V_t), and subthreshold swing (SS) [1]. This limitation has been successfully overcome by the tunnel field-effect transistor (TFET) whose working is based on band-to-band tunnelling (BTBT) phenomenon. The TFETs have been widely studied and accepted as a promising successor of the conventional MOSFET structures due to their boundless and impeccable characteristics in terms of V_t and SS. In TFETs, a gate electrode over the intrinsic layer controls the tunnelling mechanism which exhibits abrupt switching characteristics and low OFF-state current (I_{OFF}) [2]-[4]. A TFET can deliver the SS values smaller than that of a conventional MOSFET ($\sim$ 60 mV/decade at room temperature) [1]. In the recent past, several research efforts have been made to improve the performance of TFETs [5]-[13]. Despite the excellent switching performance and reduced I_{OFF}, the TFETs suffer from low ON-state current (I_{ON}) which restricts the use of TFETs for commercial applications. In order to address this issue, several modifications in the conventional TFET structure have been reported including L-channel TFET[14], U-channel TFET[15], TSR-TFET[16] and heterojunction TFETs [17]. These TFET structures are very promising for low power applications.

In order to further improve the current characteristics, in this work, a new TFET structure called dual-channel trench-gate TFET (DCTG-TFET) is proposed. The gate of the proposed device is placed in a trench to create dual channels on either side of the gate. The optimised dimensions of the proposed TFET offer significant increase in I_{ON} while keeping low I_{OFF}. This is due to simultaneous conduction of two parallel channels, low channel resistance and reduction in tunnelling width to improve the BTBT probability. In addition to large improvement in I_{ON}/I_{OFF} ratio, the proposed structure exhibits substantially lower value of SS when compared with recently reported work in the literature [14]-[16]. The proposed device is investigated and analysed using two-dimensional (2D) numerical simulations in the device simulator (ATLAS) [18].

Device Structure and Simulation Setup: The schematic 2D cross-sectional view of the proposed DCTG-TFET on silicon-on-insulator (SOI) is shown in Fig. 1. The DCTG-TFET consists of a vertical gate placed in a trench. The p^+-Si regions (doping concentration of 1×10^{20} cm^{-3}) form the source of the device on either side of the gate. The channel of the device is n-Si region having a doping concentration of 1×10^{17} cm^{-3}. The channel region is extended vertically along the gate-trench whose thickness (t_c) is optimised to 5 nm. The DCTG-TFET has two vertical drain contacts taken from n^+-Si region (doping concentration of 1×10^{19} cm^{-3}) which are isolated from the source contacts by the oxide filled in the trenches. A stacked gate oxide with a total thickness of 3 nm (1 nm SiO_2 and 2 nm HfO_2) is employed to improve the SS [19, 20]. In this study, for a fix gate height (90 nm), the source region height (h_s) and hence channel height (h_c) are varied to see their impact on the device performance. The fabrication steps of the proposed DCTG-TFET structure are similar as reported in [14, 16].

The performance of the proposed DCTG-TFET structure is evaluated using 2D numerical simulations in the ATLAS [18]. The simulations have been performed by invoking appropriate models for the TFET such as Fermi-Dirac statistics, band gap narrowing, Shockley-Read-Hall

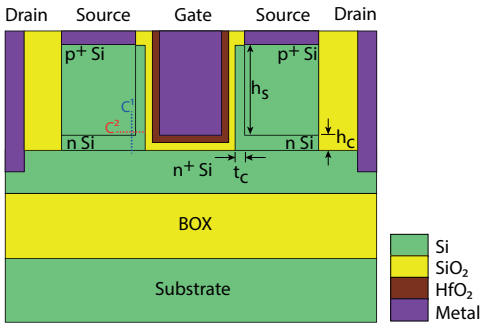

Fig. 1. Schematic cross-sectional view (not to the scale) of the DCTG-TFET

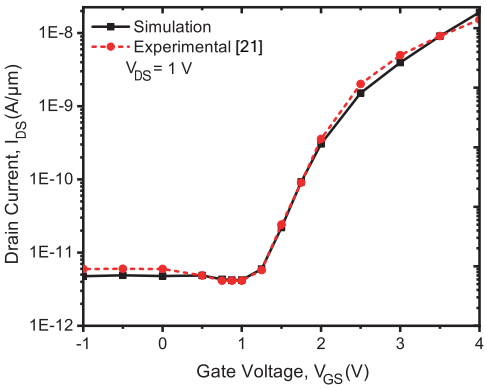

Fig. 2. Calibration of the simulation setup with pre-fabricated TFET [21]

recombination model, electric field and concentration dependent mobility Lombardi model, nonlocal BTBT model [15, 18]. In order to calibrate the simulation setup, we have simulated a pre-published fabricated TFET structure [21]. Fig. 2 gives a comparison of the simulated transfer characteristics with experimental data. As seen, there is a good agreement between simulated and measured results. Now, using above mentioned simulation models and parameters, the performance of the DCTG-TFET is analysed.

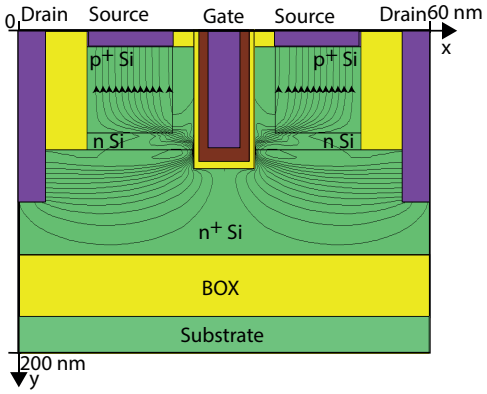

Fig. 3 *Current flow lines in the proposed DCTG-TFET for h_s = 80 nm at V_{DS} = 1 V and V_{GS} = 1.6 V*

Results & Discussion: Fig. 3 shows the current flow lines in the DCTG-TFET under ON-state condition. It can be seen that the equal amount of current flows in the device through both the channels from drain to source contacts. The parallel conduction of dual channels improves the I_{ON} of the DCTG-TFET [22, 23]. Further, it may be observed from this figure that the maximum tunnelling occurs at the corner of channel-source junction. This can be better understood from the electric field distribution at the channel-source junction as shown in Fig. 4(a). It is evident that the peak

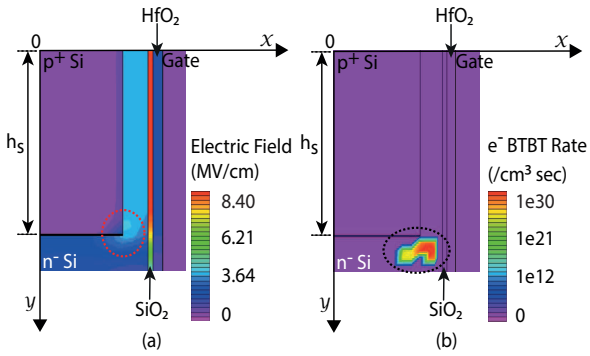

Fig. 4 *(a) 2D Electric field distribution and (b) electron BTBT rate in the DCTG-TFET for h_s = 80 nm at V_{DS} = 1 V and V_{GS} = 1.6 V*

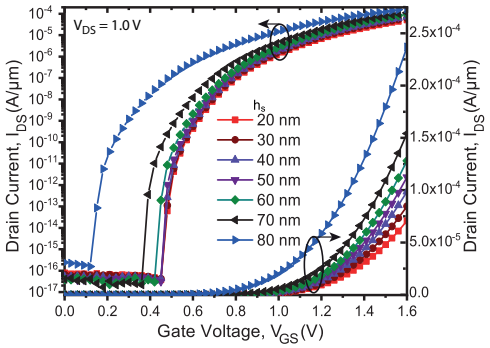

Fig. 5. Variation in transfer characteristics with h_s of DCTG-TFET

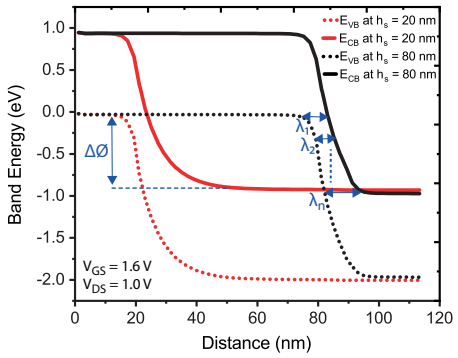

Fig. 6 *Impact of h_s on energy band diagram along the cutline C^1 in DCTG-TFET*

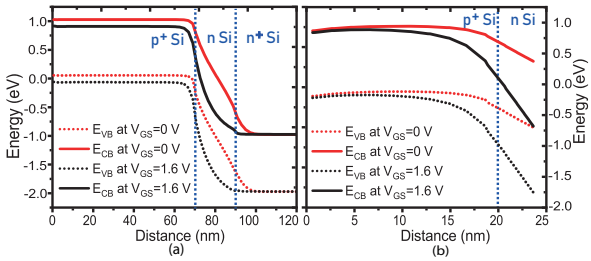

Fig. 7 *Energy band diagram for (a) cutline C^1 and (b) cutline C^2 for h_s = 80 nm at V_{DS}=1 V in DCTG-TFET*

electric field is occurring at the corner of channel-source junction leading to increase in tunnelling rate according to following equation [24]:

$$G_{BTBT} = A\varepsilon^{\sigma}\left(-\frac{B}{\varepsilon}\right) \quad (1)$$

The BTBT rate (G_{BTBT}) is reliant on the magnitude of the local electric field (ε). Where A is a constant related to the effective mass of an electron, B is tunnelling probability constant, and σ is transition constant [24]. Fig 4(b) presents the electron BTBT rate in the DCTG-TFET. As seen, the higher BTBT rate occurs at the corner of channel-source junction.

Fig. 5 gives the transfer characteristics of the DCTG-TFET for different values of h_s. It is observed that the I_{ON} improves significantly with increase in h_s. There are two-fold reasons for increase in I_{ON} of the DCTG-TFET. Firstly, for a constant gate height, h_c depends on h_s and hence channel resistance depends on h_s. As h_s is increased, the h_c decreases which reduces the channel resistance leading to improvement in I_{ON}. Secondly, the tunnelling probability increases with increase in h_s which improves the I_{ON}. This can be understood from the Wentzel-Kramer-Brillouin (WKB) approximation used to analyse the tunnelling probability (T_{WKB}) which can be written as [4]:

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\phi)}\right) \quad (2)$$

where λ represents tunnelling width, m^* is effective mass of an electron, E_g is bandgap energy, and $\Delta\phi$ is the energy range over which tunnelling can take place.

Fig. 6 demonstrates the impact of h_s on energy band diagram. It can be seen that the average tunnelling width varies with h_s while $\Delta\phi$ remains constant. To be more precise, the average tunnelling width ($\lambda_{av} = (\sum_1^n \lambda_1, \lambda_2, ..., \lambda_n)/n$) is calculated for different values of h_s which is listed in Table 1. It is clear that as h_s increases, the λ_{av} reduces which enhances the T_{WKB} leading to higher I_{ON}.

Table 1: Variation of average tunnelling width with source region height at V_{DS} = 1 V and V_{GS} = 1.6 V

$h_s(nm)$	20	30	40	50	60	70	80
$\lambda_{av}(nm)$	11.72	11.69	11.52	11.23	10.84	9.91	7.55

Further, for a fixed value of V_{DS}, the impact of V_{GS} on I_{DS} (Fig. 5) is explained by the energy band diagrams as shown in Fig. 7. In Fig. 7(a), the energy band diagram is plotted at cutline C^1 which illustrates that the tunnelling width reduces with increase in V_{GS}, leading to higher I_{ON}. On the other hand, Fig. 7(b) shows the energy band diagram at cutline C^2. It is evident that at V_{GS} = 0 V, there is no overlap between valence band energy (E_{VB}) and conduction band energy (E_{CB}). Whereas, at V_{GS} = 1.6 V, there is significant overlap between E_{VB} and E_{CB} and hence a part of I_{ON} flows laterally at channel-source corner under the ON-state condition (as seen in Fig. 3).

Fig. 8 demonstrates the variation of I_{ON}/I_{OFF} ratio and λ_{av} as a function of h_s. It is observed from the figure that λ_{av} decreases with increase in h_s, as a result the I_{ON}/I_{OFF} ratio improves upto h_s = 70 nm. However, the I_{ON}/I_{OFF} ratio degrades after h_s = 70 nm due to increase in I_{OFF}. Therefore, the optimum value of h_s is 70 nm for the proposed DCTG-TFET.

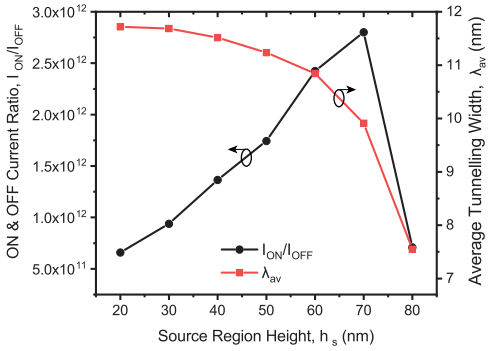

Fig. 8 *Impact of h_s on I_{ON}/I_{OFF} ratio and λ_{av} at V_{DS} = 1 V and V_{GS} = 1.6 V in DCTG-TFET*

In addition to the improvement in I_{ON}, the proposed DCTG-TFET structure provides significant low value of SS with reasonable V_t. Fig. 9 shows the effect of h_s on V_t and SS. It is seen that both V_t and SS reduce with increase in h_s due to rapid increase in drain current.

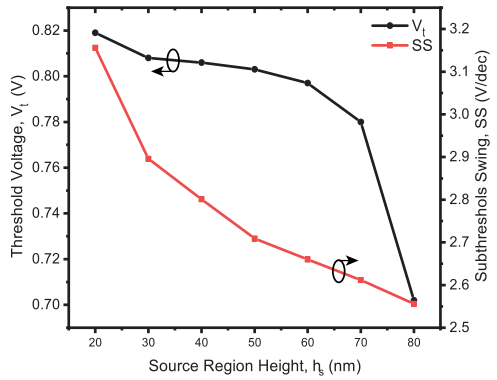

Fig. 9 *Variation of V_t and SS with h_s at V_{DS} = 1 V and V_{GS} = 1.6 V in DCTG-TFET*

Table 2 gives a comparison of proposed DCTG-TFET performance parameters with other reported TFET structures in literature. It is observed that the proposed DCTG-TFET provides about five times higher I_{ON} as compared to recently reported TSR-TFET. The proposed device exhibits one order of magnitude improvement in I_{ON}/I_{OFF} ratio. Moreover, the DCTG-TFET gives extremely low value of SS (3.77 mV/dec) which is seventeen times lower than that of the TSR-TFET.

Table 2: Performance parameter comparison of DCTG-TFET with other reported TFETs

Performance Parameter	L-TFET [14]	U-TFET [15]	TSR-TFET [16]	DCTG-TFET [This work]
V_t (V)	0.45	1.04	0.23	0.72
I_{ON} (μA/μm)	0.47	0.28	10.3	57.4
I_{ON}/I_{OFF}	$\sim 10^5$	$\sim 10^7$	$\sim 10^{10}$	$\sim 10^{11}$
SS (mV/dec)	34	33.8	66.25	3.77

Conclusion: A new TFET structure having a gate placed in a vertical trench is presented. The enhancement in drive current is obtained due to parallel conduction of dual channels, reduction in channel resistance and decrease in tunnelling width. The increased drive current has been justified with the help of electric field distribution, BTBT rate and energy band diagrams. The I_{ON}/I_{OFF} ratio of the DCTG-TFET is $\sim 10^{11}$ which is significantly higher as compared to the recently reported TFETs. Moreover, the proposed device exhibits extremely low value of SS (3.77 mV/dec). The impact of h_s has been studied on the performance of DCTG-TFET and the optimum value of h_s is found as 70 nm. The simulation results reveal that the DCTG-TFET is an attractive choice for low power switching applications.

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